Application Note

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Document No.: AN1113

APM32F003x4x6 Hardware Development Guide

Version: V1.0

1 Introduction

This application note is a minimum design specification for system hardware of the APM32F003x4x6 series, including power supply scheme, clock source, reset mode, startup mode settings, and debugging management.

The detailed reference design drawing is also included in this document, including descriptions of main components, interfaces, and modes.

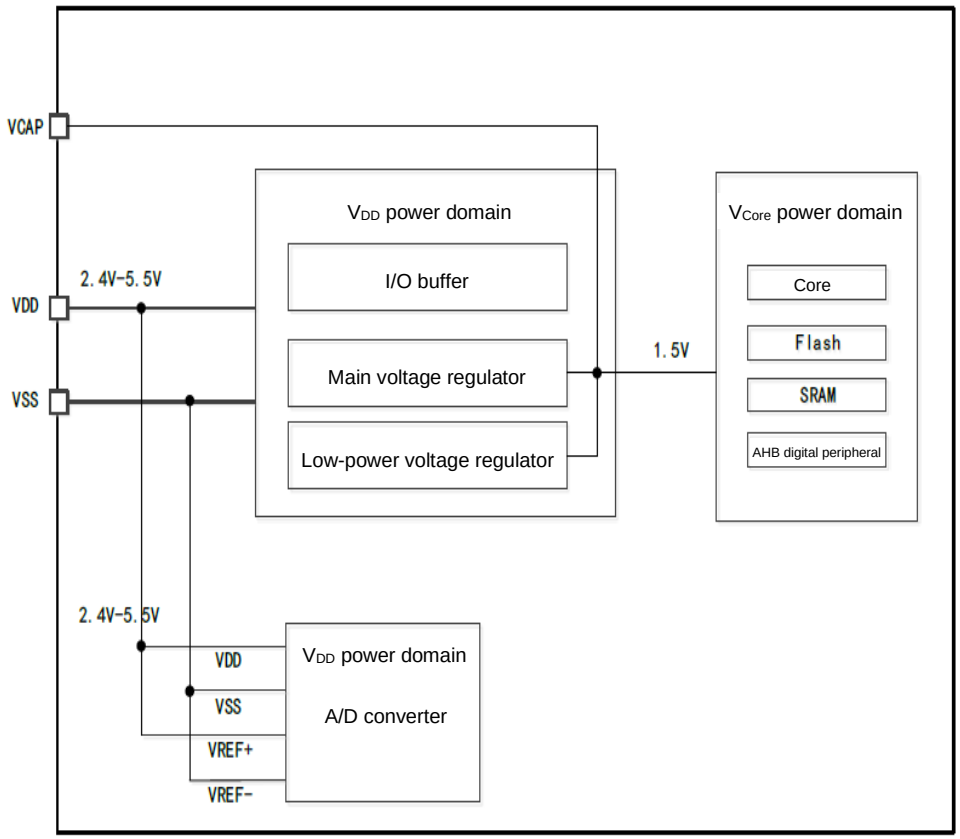
Contents

2 Power supply

2.1 Introduction

The power supply is the foundation for stable operation of a system, with an operating voltage of 2.4 ~ 5.5V for the main power supply, and 1.5V power supply can be provided by the internal main voltage regulator and the low-power voltage regulator.

Figure 1 Power Supply Control Structure Block Diagram



2.1.1 V_{DD} power domain

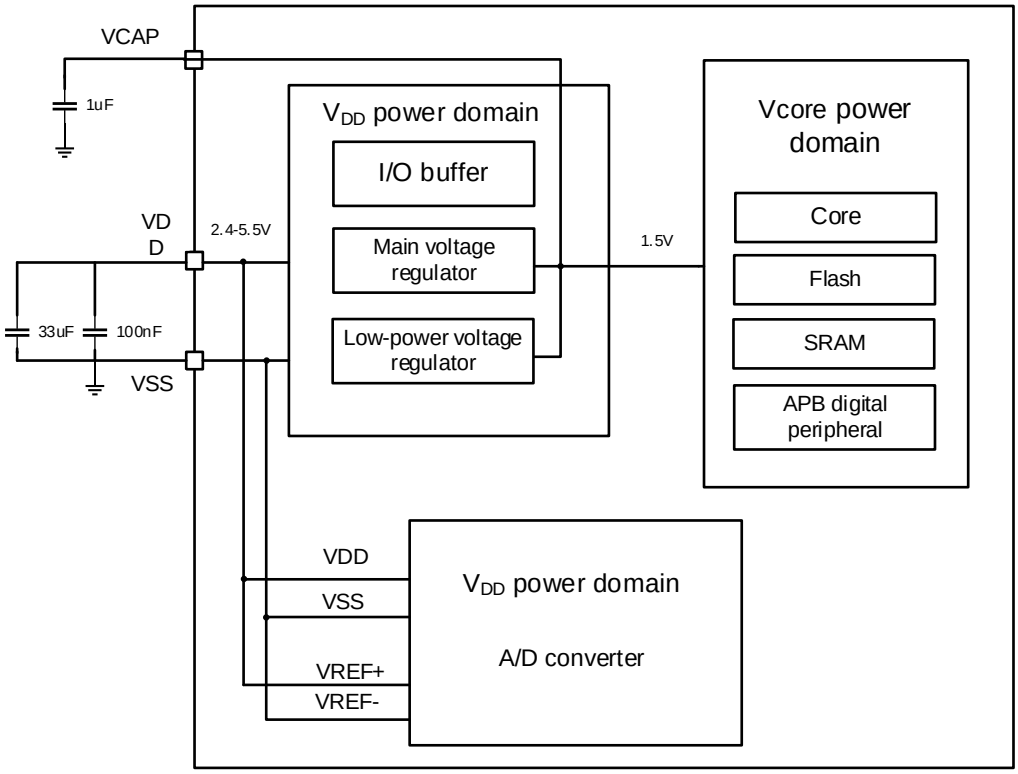
The V_{DD}/V_{SS} pin can supply power to the internal main voltage regulator (MVR), internal low-power voltage regulator (LPVR), and I/O ports, within the voltage range of 2.4~5.5V.

2.1.2 V_{Core} field

The main voltage regulator and low-power voltage regulator together supply power to the core, FLASH, RAM, and digital peripherals, with a supply voltage of 1.5V.

2.2 Power supply scheme

Figure 2 Power Supply Scheme



Pay attention to the power supply range of each power domain:

Table 1Power Supply Scheme

Name	Voltage range	Description
V_{DD}	2.4 ~ 5.5V	VDD directly supplies power to the IO port and the internal voltage regulator.
V_{core}	1.5V	1.5V power supply is provided to the core, Flash, and SRAM through the internal voltage regulator.

Where:

Table 2 Precautions for Power Domain

V_{DD}	V_{DD} must be connected to V_{DD} power supply of an external capacitor (a 100nF ceramic capacitor (1) and a tantalum capacitor not less than 4.7μF).
V_{CAP}	The stability of the main voltage regulator is achieved by connecting the external capacitor C_{EXT} to the VCAP pin. When the voltage regulator is enabled, the pin VCAP must be connected to a ceramic capacitor with a rated capacitance of 1 μF and low ESR (1).

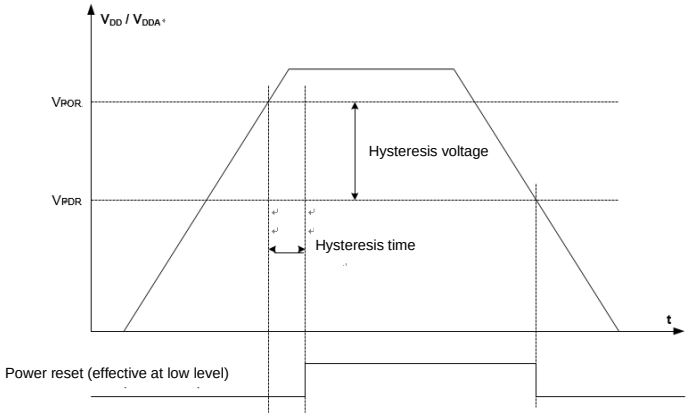
(1) It is recommended to use the ceramic capacitors made of X7R

2.3 Power Management and Reset

2.3.1 Power-on reset and power-down reset (POR and PDR)

When the VDD is lower than the threshold voltage $_{VPOR}$ and $_{VPDR}$, the chip will automatically remain in the reset state. The waveform diagrams of power-on reset and power-down reset are as follows. For POR, PDR, hysteresis voltage and hysteresis time, please refer to the *Datasheet*.

Figure 3Power-on Reset and Power-down Reset Oscillogram



2.3.2 System reset

The system reset source is divided into external reset source and internal reset source.

Table 3 Reset Source

External reset source:	Low level on NRST pin.
Internal reset source:	(1) Window watchdog termination count (WWDT reset) (2) Independent watchdog termination count (IWDT reset) (3) Software reset (SW reset) (4) Power-on reset (POR)/Power-down reset (PDR) (5) CPU software reset (6) EMC reset

A system reset will occur when any of the above events occurs. Besides, the reset event source can be identified by viewing the reset flag bit in RCM_CSTS (control/status register).

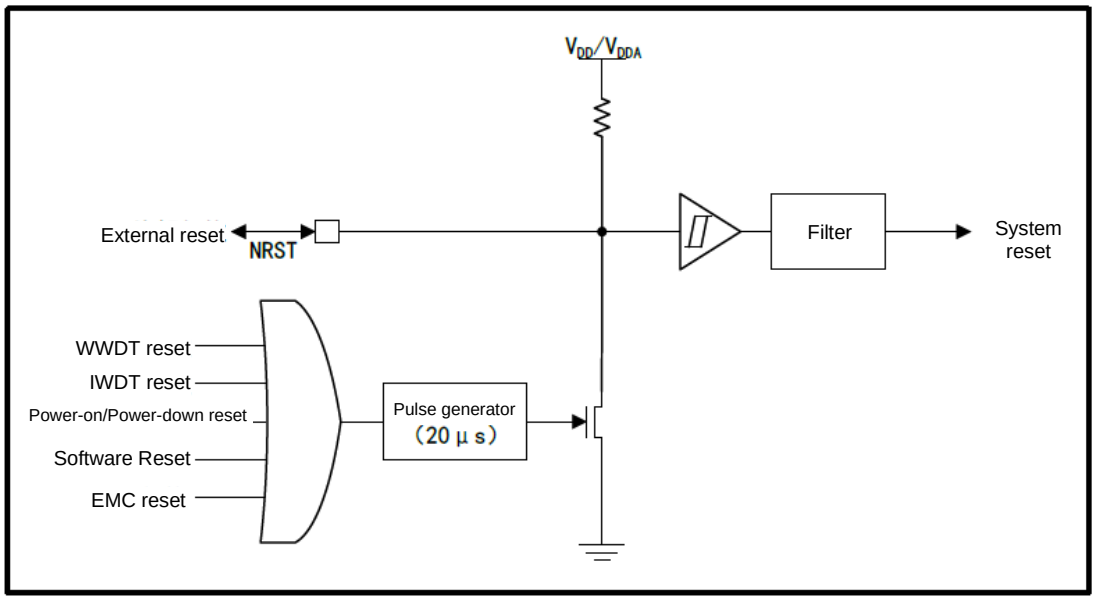
2.3.1.1 System reset circuit

The reset source is used in the NRST pin, which remains low in reset process. The internal reset source generates a pulse with a delay of at least 20μs on the NRST pin through the

pulse generator, which causes the NRST to maintain the level and generate reset; the external reset source directly pulls down the NRST pin level to generate reset.

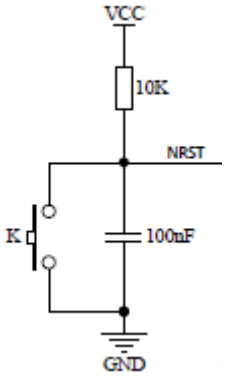
The system reset circuit is shown in Figure 5:

Figure 4 System Reset Circuit



Recommend external reset circuit

Figure 5 External Reset Circuit

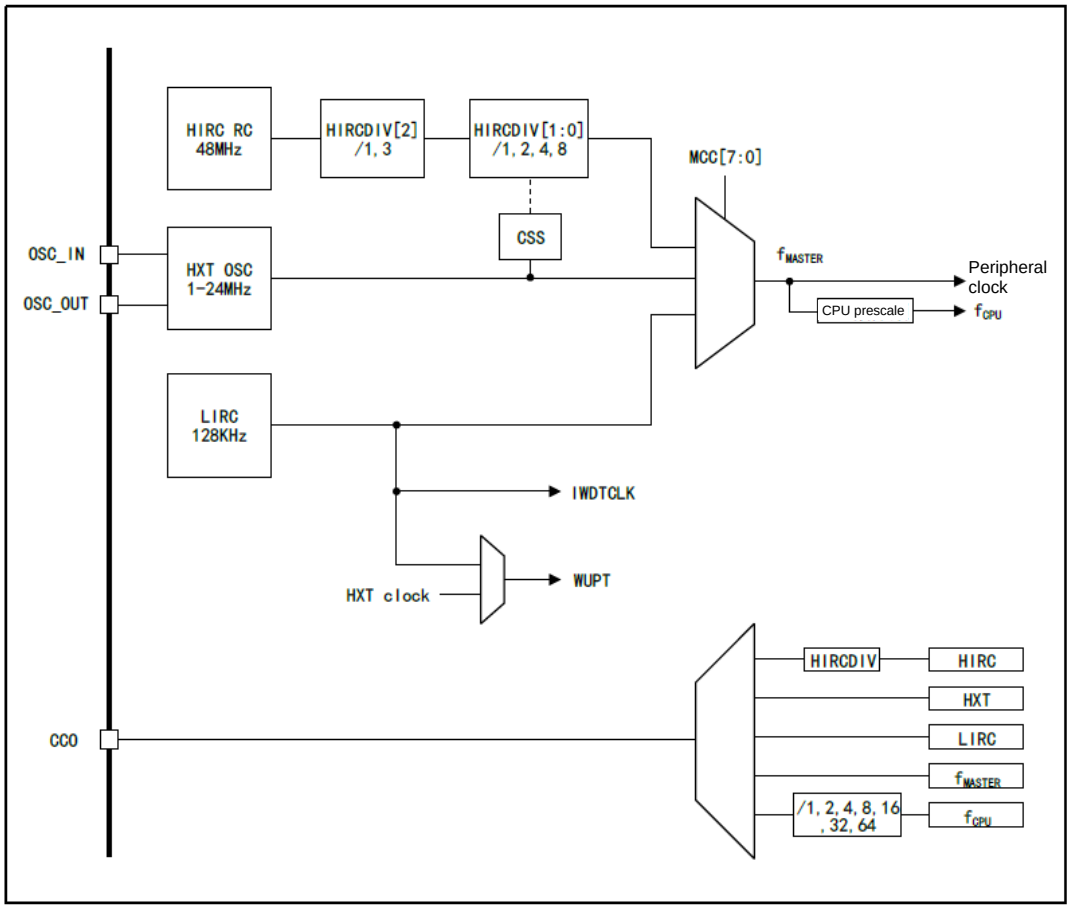


3 Clock

The clock sources of the entire system include HXT, HIRC, and LIRC. For the characteristics of the clock source, please refer to the relevant chapter of "Electrical Characteristics" in the datasheet.

Clock tree:

Figure 6 Clock Tree



3.1 External clock source

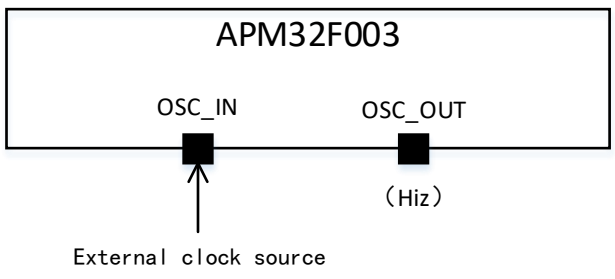
The external clock signal is HXT (high-speed external clock signal).

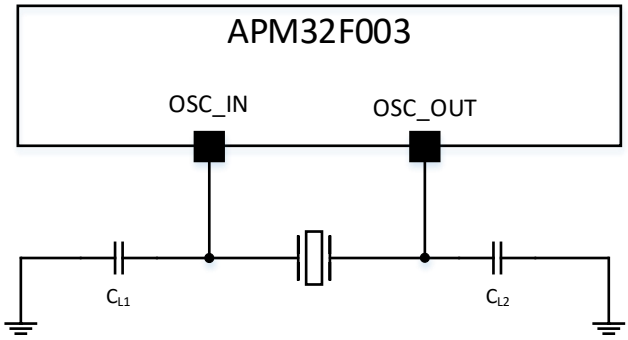
There are two kinds of external clock sources:

- External clock of user
- External crystal/ceramic resonator

The hardware configuration of the two kinds of clock sources is shown in the figure below.

Table 4 HXT Clock Source Hardware Configuration

Clock source	Hardware configuration
External clock	

Clock source	Hardware configuration
Crystal/Ceramic resonator	

(1) In order to reduce the distortion of clock output and shorten the startup stabilization time, the crystal/ceramic resonator and load capacitor must be as close to the oscillator pin as possible. The value of the matching capacitance (C_{L1}, C_{L2}) must be adjusted according to the selected oscillator.
(2) The load capacitor C_L follows the formula of: $C_L=C_{L1} \times C_{L2} / (C_{L1}+C_{L2}) + C_S$. C_S is relevant capacitance of PCB and MCU pins. The typical value is between 2pF and 10pF.

3.1.1 HXT high-speed external clock signal

HXT clock signal is generated by HXT external crystal/ceramic resonator and HXT external clock sources.

Table 5 Clock Source Generating HXT

Name	Description
External clock source (HXT bypass)	Provide clock to the MCU through OSC_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the maximum frequency is up to 24MHz. In hardware connection, it must be connected to the OSC_IN pin and the OSC_OUT pin must be suspended.
External crystal/ceramic resonator (HXT crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency range is 1~24MHz. OSC_IN, OSC_OUT is required to connect the resonator, and it can be turned on and off by setting the HXTEN bit in RCM_ECC in the clock control register. Regarding the size of the external matching capacitor, please refer to the formula: $C_{L1}= C_{L2} = 2*(C_L- C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, and the typical value is 10pF. When selecting an external high-speed crystal resonator, it is

Name	Description
	recommended to select the one with a load capacitance of around 20pF, so that the external matching capacitors (1) C_{L1} and C_{L2} only need to have a capacitance value of 20pF, and the PCB should be as close as possible to the crystal oscillator pins.

(1) It is recommended to use the temperature compensation capacitors made of NPO (COG) for the matching capacitor of the crystal oscillator.

4 Debugging interface (SW-DP)

The product supports serial debugging interface (SWD).

Table 6 Debugging Interface

Name	Description
SW-DP	SW-DP interface provides 2-pin (data + clock) interface for AHB module.

4.1 Debugging Pin Function Configuration

- Realize the on-line programming and debugging of the chip.
- Use KEIL/IAR and other software to implement on-line debugging, downloading and programming.
- Flexible implementation of production of bus-off programmer.

Table 7 Pin Function Configuration

JTAGDIS	Configured as dedicated pin for debugging	I/O port assignment of SWD interface	
		PD1/SWDIO	PD2/SWCLK
0	SW-DP interface is enabled	SWDIO	SWCLK
1	SW-DP interface is disabled	GPIO	GPIO

4.2 IO status during reset and just after reset

If the multiplexing function is not enabled during and just after GPIO reset, the I/O port will be configured as floating input mode, and in such case, the pull-up/pull-down resistor is disabled in input mode. After reset, all pins except for debugging interfaces PD1 and PD2 are in floating input mode. The debugging pins PD1 and PD2 are set as multiplexing function:

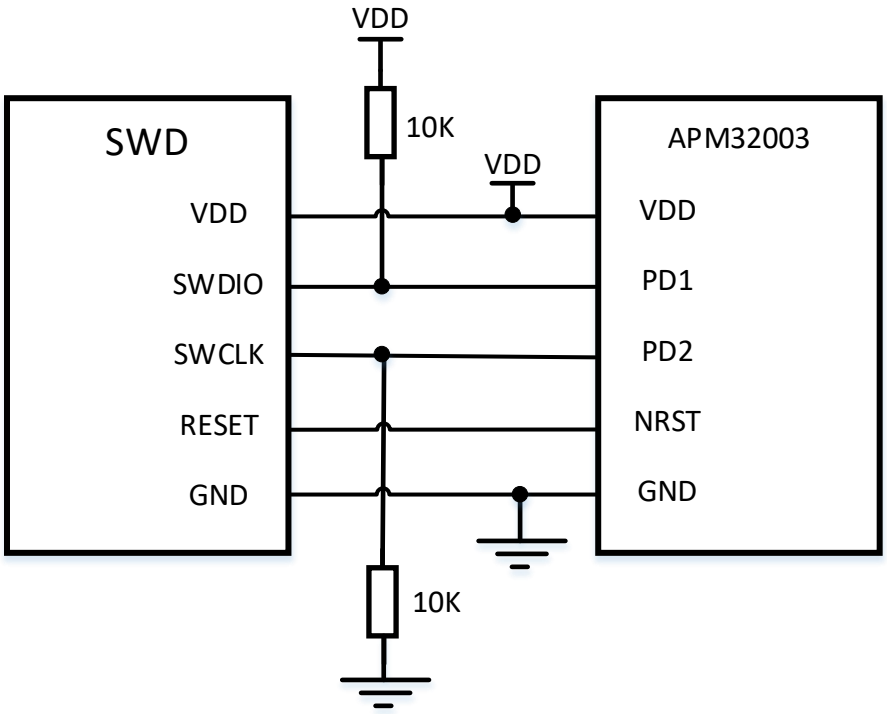
- PD2: SWCLK is set to pull-down mode;
- PD1: SWDIO is set to pull-up mode;

When the debugging function is disabled, it serves as an ordinary GPIO pin.

4.3 Recommended Debugging Interface Circuit

Recommended SWD interface reference design:

Figure 7 SWD Interface Circuit



Note:

(1) The reference design for the SWD interface is to add an external pull-up resistor and pull-down resistor to the SWDIO and SWCLK pins, which can enhance the anti-interference ability of downloading and debugging. If these two pins are multiplexed for other functions, please evaluate the impact of the pull-up and pull-down resistors and make adjustments according to the actual situation.

5 Design Suggestions

5.1 PCB Stacking

- Number of layers: It is recommended to use the multi-layer design to ensure independent GND and power layers, which can better ensure signal integrity and enhance shielding effect. However, considering the costs, users can reduce the

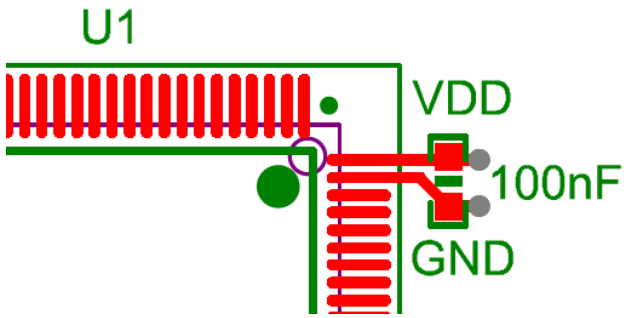
number of stacking layers while ensuring good grounding and power supply.

- Signal and formation: The signal layer should be adjacent to the formation. This helps to reduce the electromagnetic interference and the loop area of the signal path, and can serve as a reference plane for the signal.
- Power supply and formation: The power supply layer should be separated from the formation.

5.2 Power Supply Design

- Stable power input: Ensure stable power supply and filter the power noise.
- Decoupling capacitors: Place one or more 100nF decoupling capacitors at the VDD pin near the chip.

Figure 8 Recommended Power Pin Decoupling Capacitor Layout Design

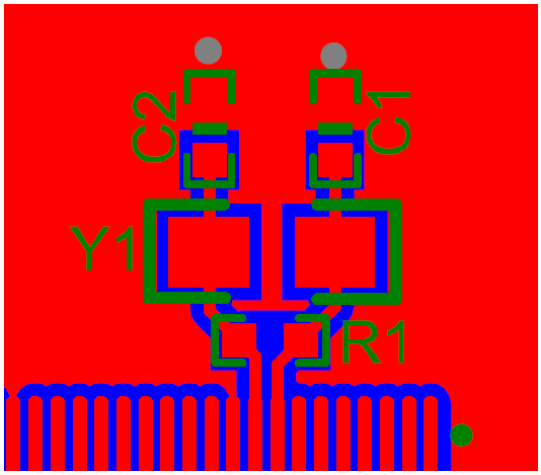


- Power supply wiring: It is recommended that the power supply wiring should be wide and short enough to reduce the influence of parasitic parameters and the voltage drop.

5.3 Clock Design

- Crystal oscillator selection: Choose an appropriate crystal oscillator and ensure it meets the operating frequency and stability requirements of the MCU.
- Wiring suggestions: Clock signal wiring should be as short as possible and be away from strong interference signals such as high current and high-speed signal lines. It is recommended to use package processing to enhance the shielding effect.
- Layout suggestions: The crystal oscillator circuit should be placed close to the chip, and to reduce the interference, it is best to ensure a complete ground plane below the entire crystal oscillator circuit.

Figure 9 Recommended Clock Pin Layout Design



5.4 I/O Design

- I/O configuration: Correctly configure the modes of I/O ports, such as input, output, pull-up and pull-down, and open-drain mode.
- Protection: For externally connected I/O ports, consider adding the voltage protection (TVS tube) and series resistor.

5.5 EMC and EMI

- Layout: Consider the design of electromagnetic compatibility (EMC) and electromagnetic interference (EMI), and the layout should be reasonable. For example, keep the MCU away from high-power and strong interference sources, and consider how to reduce the loop area, etc.
- Shielding: Use shielding and reasonable grounding strategies for sensitive and high-speed circuits.

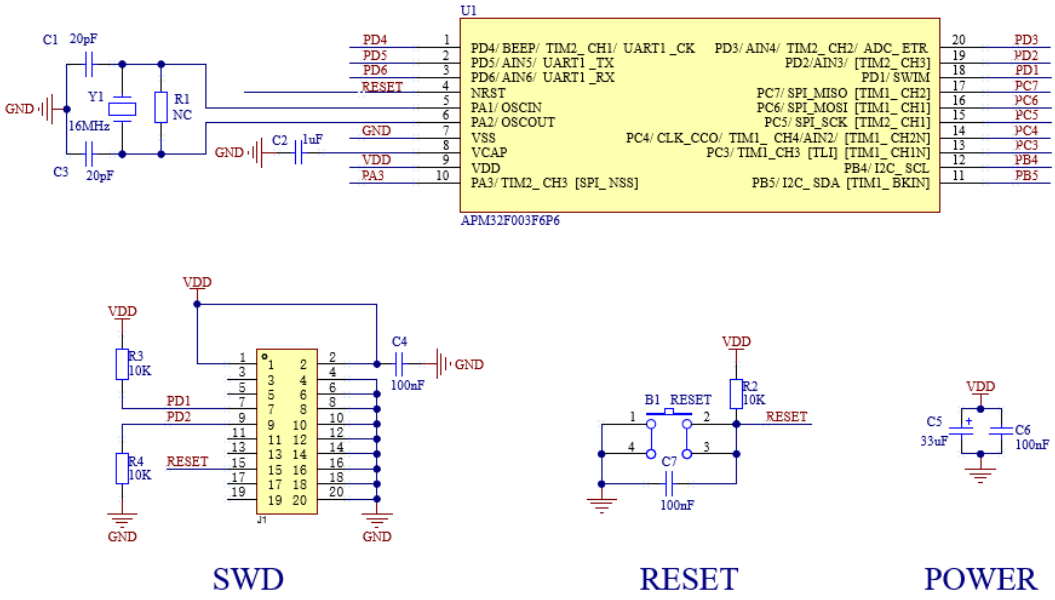
5.6 Grounding

- Single-point grounding: In low-frequency circuits or circuits with not high noise requirements, adopting single-point grounding can avoid formation of ground loop. In such case, all grounding points should be connected to a common grounding point, which is usually the negative pole of the power supply or some grounding plane on the circuit board.
- Multi-point grounding: In high-frequency circuits or high-current circuits, usually multi-point grounding is used. The grounding of each component or function module is directly connected to the nearest grounding plane, which can reduce the impedance of the ground wire, and reduce the noise and electromagnetic interference.

- Separation of analog from digital ground: If the MCU processes the analog and digital signals simultaneously, the analog ground and digital ground should be processed separately. This can be achieved by physically separating two ground planes and merging them at a certain point to connect them to the main ground, which can reduce the interference of digital noise with the analog signals.

5.7 Reference Schematic Diagram Design

Figure 10 Reference Schematic Diagram



SWD RESET POWER

6 Revision history

Table 8 Document Revision History

Date	Version	Revision History
July, 2024	V1.0	New edition

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